CLAIMS

1. A circuit comprising:

a database configured to store a pointer for each first parameter of a network protocol; and

a processing circuit configured to (i) process at least one of said first parameters in an incoming packet in accordance with said pointer to produce a second parameter and (ii) present an outgoing packet containing said second parameter.

2. The circuit according to claim 1, wherein said database is further configured to store an offset and a length for each said first parameter, and said processing circuit is further configured to partition said incoming packet in accordance with said offsets and said lengths to extract said first parameters.

3. The circuit according to claim 2, further comprising an interface configured to download said offsets, said lengths, and said pointers for storage in said database.

4. The circuit according to claim 1, wherein said processing circuit comprises:

a parsing circuit configured to partition said incoming packet;

a plurality of peripheral blocks each (i) linked to said pointers and (ii) configured to perform a process involving said first parameters; and

an assembling circuit configured to generate said outgoing packet.

5. The circuit according to claim 4, wherein said database is further configured to store a second offset, and a second length for each said second parameter of a second network protocol.

6. The circuit according to claim 4, further comprising an interface connectable to a peripheral block external to said circuit.

7. The circuit according to claim 4, wherein said peripheral blocks are at least two circuits of a content addressable memory circuit, a time to live circuit, a comparison circuit, a counter circuit, a value swapping circuit, a stuffing circuit, a de-stuffing circuit, a cyclic redundancy checksum circuit, a parity circuit, a first-in-first-out circuit, a length construction generator circuit, a header error control synchronization circuit, a frame relay lookup circuit, a data link connection identifier circuit, a protocol identification analysis circuit, a point-to-point protocol verification circuit, a parameter discard circuit, and a buffer circuit.

8. The circuit according to claim 4, wherein at least one peripheral block is configured to simultaneously processes a plurality of first parameters.

9. The circuit according to claim 1, wherein said processing circuit is configured as only hardware.

10. An assembly comprising:

a first circuit configured to delineate a receive frame from a first network having a network protocol to produce an incoming packet;

a second circuit configured to (i) store a pointer for each first parameter of said network protocol, (ii) process at least one first parameter in said incoming packet in accordance with said pointer to produce a second parameter, and (iii) present an outgoing packet containing said second parameter; and

a third circuit configured to frame said outgoing packet to present a transmit frame to a second network.

11. The assembly according to claim 10, wherein said second circuit is further configured to store an offset and a length for each said first parameters and partition said incoming packet in accordance with said offsets and said lengths to extract said first parameters from said incoming packet.

12. The assembly according to claim 10, wherein said first circuit is further configured to provided a plurality of frame delineation methods for a plurality of network protocols.

13. The assembly according to claim 12, further comprising an interface configured to permit a selection among said frame delineation methods.

14. The assembly according to claim 10, wherein said second circuit is further configured to provided a plurality of framing methods for a plurality of network protocols.

15. The assembly according to claim 14, further comprising an interface configured to permit a selection among said framing methods.

16. The assembly according to claim 10, wherein said third circuit is further configured to delineate a second receive frame from said second network to produce said incoming packet.

17. The assembly according to claim 16, wherein said first circuit is further configured to frame said outgoing packet to present a second transmit frame to said first network.